

Notice of Allowability	Application No.	Applicant(s)	
	09/944,085	INUKAI ET AL.	
	Examiner	Art Unit	
	Leonid Shapiro	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to RCEX, filed on 01/27/05.
2. ☒ The allowed claim(s) is/are 1-45.
3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☒ All b) ☐ Some* c) ☐ None of the:
 1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
 - * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
 5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|--|
| <ol style="list-style-type: none"> 1. <input type="checkbox"/> Notice of References Cited (PTO-892) 2. <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) 3. <input checked="" type="checkbox"/> Information Disclosure Statements (PTO-1449 or PTO/SB/08),
Paper No./Mail Date _____ 4. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit
of Biological Material | <ol style="list-style-type: none"> 5. <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) 6. <input type="checkbox"/> Interview Summary (PTO-413),
Paper No./Mail Date _____ 7. <input type="checkbox"/> Examiner's Amendment/Comment 8. <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance 9. <input type="checkbox"/> Other _____ |
|--|--|

Allowable Subject Matter

1. Claims 1-45 are allowed.
2. The following is a statement of reasons for the indication of allowable subject matter:

The invention concerns a method of driving an EL display device including a plurality of pixels, each having a first TFT, a second TFT, a third TFT, and an organic EL element, the method comprising:

dividing a frame period into $n + m$ display periods with n and m being natural numbers of one or more, wherein the $n + m$ display periods each correspond to one bit of a digital video signal among n bits of the digital video signal, a plurality of display periods, among the $n + m$ display periods correspond to the same bit of the digital video signal, and other display periods corresponding to other bits of the digital video signal, among the $n + m$ display periods, appear between the plurality of display periods;

for each of the $n + m$ display periods, inputting the corresponding bit of the digital video signal to a gate electrode of the second TFT by turning on the first TFT and beginning the respective display period by turning off the third TFT; and

after each of the $n+m$ display period begins completing the respective display period by turning on the third TFT;

wherein the organic EL element emits light when the second TFT is turned on, and does not emit light when the second TFT is turned off,

wherein the first TFT comprises a crystalline semiconductor film, a gate insulating film over the crystalline semiconductor film, first and second gate electrodes formed over the crystalline semiconductor film with the gate insulating film interposed therebetween, and first and second channel forming regions in the crystalline semiconductor film below the first and second gate electrodes, respectively, and a pair of first impurity regions in the crystalline semiconductor film between the first and second channel forming regions and a third impurity region between the pair of first impurity regions, as disclosed in claim 1. The

closest art, Someya, Kane, and Naka disclosed related displays, either singularly or in combination fail to anticipate or render the above underlined limitations obvious.

The invention also concerns a method of driving an EL display device including a plurality of pixels, each having a first TFT, a second TFT, a third TFT, and an organic EL element, the method comprising:

dividing a frame period into $n + m$ display periods with n and m being natural numbers of one or more, wherein the $n + m$ display periods each correspond to one bit of a digital video signal among n bits of the digital video signal, a plurality of display periods, among the $n + m$ display periods correspond to the most significant bit of the digital video signal, and other display periods corresponding to other bits of the digital video signal, among the $n + m$ display periods, appear between the plurality of display periods;

for each of the $n + m$ display periods, inputting the corresponding bit of the digital video signal to a gate electrode of the second TFT by turning on the first TFT and beginning the respective display period by turning off the third TFT; and

after each of the $n+m$ display period begins completing the respective display period by turning on the third TFT;

wherein the organic EL element emits light when the second TFT is turned on, and does not emit light when the second TFT is turned off,

wherein the first TFT comprises a crystalline semiconductor film, a gate insulating film over the crystalline semiconductor film, first and second gate electrodes formed over the crystalline semiconductor film with the gate insulating film interposed therebetween, and first and second channel forming regions in the crystalline semiconductor film below the first and second gate electrodes, respectively, and a pair of first impurity regions in the crystalline semiconductor film between the first and second channel forming regions and a third impurity region between the pair of first impurity regions, as disclosed in claim 5. The

closest art, Someya, Kane, and Naka disclosed related displays, either singularly or in combination fail to anticipate or render the above underlined limitations obvious.

The invention is also concerns a method of driving an EL display device including a plurality of pixels, each having a first TFT, a second TFT, a third TFT, and an organic EL element, the method comprising:

dividing a frame period into $n + m$ display periods with n and m being natural numbers of one or more, wherein the $n + m$ display periods each correspond to

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one bit of a digital video signal among n bits of the digital video signal, upper bits of the digital video signal correspond to a plurality of display periods, among the $n + m$ display periods correspond to the same bit of the digital video signal, and other display periods corresponding to other bits of the digital video signal, among the $n + m$ display periods, appear between the plurality of display periods;

for each of the $n + m$ display periods, inputting the corresponding bit of the digital video signal to a gate electrode of the second TFT by turning on the first TFT and beginning the respective display period by turning off the third TFT; and

after each of the $n+m$ display period begins completing the respective display period by turning on the third TFT;

wherein the organic EL element emits light when the second TFT is turned on, and does not emit light when the second TFT is turned off,

wherein the first TFT comprises a crystalline semiconductor film, a gate insulating film over the crystalline semiconductor film, first and second gate electrodes formed over the crystalline semiconductor film with the gate insulating film interposed therebetween, and first and second channel forming regions in the crystalline semiconductor film below the first and second gate electrodes, respectively, and a pair of first impurity regions in the crystalline semiconductor film between the first and second channel forming regions and a third impurity region between the pair of first impurity regions, as disclosed in claim 9. The

closest art, Someya, Kane, and Naka disclosed related displays, either singularly or in combination fail to anticipate or render the above underlined limitations obvious.

The invention is also concerns a method of driving an EL display device including a plurality of pixels, each having a first TFT, a second TFT, a third TFT, and an organic EL element, the method comprising:

dividing a frame period into $n + m$ display periods with n and m being natural numbers of one or more, wherein the $n + m$ display periods each correspond to one bit of a digital video signal among n bits of the digital video signal, a plurality of display periods, among the $n + m$ display periods correspond to the same bit of the digital video signal, and other display periods corresponding to other bits of the digital video signal, among the $n + m$ display periods, appear between the plurality of display periods;

for each of the $n + m$ display periods, inputting the corresponding bit of the digital video signal to a gate electrode of the second TFT by turning on the first TFT and beginning the respective display period by turning off the third TFT; and

after each of the $n+m$ display period begins completing the respective display period by beginning another display period;

wherein the organic EL element emits light when the second TFT is turned on, and does not emit light when the second TFT is turned off,

wherein the first TFT comprises a crystalline semiconductor film, a gate insulating film over the crystalline semiconductor film, first and second gate electrodes formed over the crystalline semiconductor film with the gate insulating film interposed therebetween, and first and second channel forming regions in the crystalline semiconductor film below the first and second gate electrodes,

respectively, and a pair of first impurity regions in the crystalline semiconductor film between the first and second channel forming regions and a third impurity region between the pair of first impurity regions, as disclosed in claim 13. The closest art, Someya, Kane, and Naka disclosed related displays, either singularly or in combination fail to anticipate or render the above underlined limitations obvious.

The invention is also concerns a method of driving an EL display device including a plurality of pixels, each having a first TFT, a second TFT, a third TFT, and an organic EL element, the method comprising:

dividing a frame period into $n + m$ display periods with n and m being natural numbers of one or more, wherein the $n + m$ display periods each correspond to the most significant bit of a digital video signal among n bits of the digital video signal, a plurality of display periods, among the $n + m$ display periods correspond to the same bit of the digital video signal, and other display periods corresponding to other bits of the digital video signal, among the $n + m$ display periods, appear between the plurality of display periods;

for each of the $n + m$ display periods, inputting the corresponding bit of the digital video signal to a gate electrode of the second TFT by turning on the first TFT and beginning the respective display period by turning off the third TFT; and

after each of the $n+m$ display period begins completing the respective display period by beginning another display period;

wherein the organic EL element emits light when the second TFT is turned on, and does not emit light when the second TFT is turned off,

wherein the first TFT comprises a crystalline semiconductor film, a gate insulating film over the crystalline semiconductor film, first and second gate electrodes formed over the crystalline semiconductor film with the gate insulating film interposed therebetween, and first and second channel forming regions in the crystalline semiconductor film below the first and second gate electrodes, respectively, and a pair of first impurity regions in the crystalline semiconductor film between the first and second channel forming regions and a third impurity region between the pair of first impurity regions, as disclosed in claim 17. The closest art, Someya, Kane, and Naka disclosed related displays, either singularly or in combination fail to anticipate or render the above underlined limitations obvious.

The invention is also concerns a method of driving an EL display device including a plurality of pixels, each having a first TFT, a second TFT, a third TFT, and an organic EL element, the method comprising:

dividing a frame period into $n + m$ display periods with n and m being natural numbers of one or more, wherein the $n + m$ display periods each correspond to one bit of a digital video signal among n bits of the digital video signal, upper bits of the digital video signal correspond to a plurality of display periods, among the $n + m$ display periods, and other display periods corresponding to other bits of the digital video signal, among the $n + m$ display periods, appear between the plurality of display periods;

for each of the $n + m$ display periods, inputting the corresponding bit of the digital video signal to a gate electrode of the second TFT by turning on the first TFT and beginning the respective display period by turning off the third TFT; and

after each of the n+m display period begins completing the
respective display period by beginning another display period;

wherein the organic EL element emits light when the second TFT is
turned on, and does not emit light when the second TFT is turned off,

wherein the first TFT comprises a crystalline semiconductor film, a
gate insulating film over the crystalline semiconductor film, first and second gate
electrodes formed over the crystalline semiconductor film with the gate insulating
film interposed therebetween, and first and second channel forming regions in
the crystalline semiconductor film below the first and second gate electrodes,
respectively, and a pair of first impurity regions in the crystalline semiconductor
film between the first and second channel forming regions and a third impurity
region between the pair of first impurity regions, as disclosed in claim 21. The
closest art, Someya, Kane, and Naka disclosed related displays, either singularly or in
combination fail to anticipate or render the above underlined limitations obvious.

Any comments considered necessary by applicant must be submitted no later
than the payment of the issue fee and, to avoid processing delays, should preferably
accompany the issue fee. Such submissions should be clearly labeled "Comments on
Statement of Reasons for Allowance."


Telephone inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 571-272-7683. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LS
09.14.05



VIJAY SHANKAR
PRIMARY EXAMINER